INVENTATEQ
LEARN SKILLS • GET PLACED

MASTER SYSTEM VERILOG COURSE With Placement

Build In-Demand Professional Expertise with Real-Time Hands-on System Verilog Training

BEST RATED ON TOP PLATFORMS

Google Reviews ★★★★★ · Trustpilot ★★★★★ · Sulekha ★★★★★

COURSE BENEFITS

- ✓ 100% Practical & Real-Time Hands-on Labs
- ✓ End-to-End Capstone Implementation Projects
- ✓ Industry Recognized Certification Preparation
- ✓ 100% Dedicated Placement Support in MNC's & Mock Interviews

15+	500+	25K	15K
YEARS OF EXCELLENCE	HIRING PARTNERS	STUDENTS TRAINED	STUDENTS PLACED

Chat on WhatsApp
FREE Career Counselling
+91 85500 00909

YOUR FUTURE
STARTS HERE !

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ARE YOU FACING THESE CHALLENGES ?

TOO MUCH THEORY
NO PROJECTS
SKILL GAP
NO GUIDANCE
?

- Still searching for your first job after graduation?
- Worried about the Gap? And don't know how to start your career?
- Stuck in a low-salary job? and seeking for better growth opportunities?
- Fear of switching to an IT career from a non-IT background
- Not getting interview calls despite applying to 100+ jobs?

How Inventateq Helps You

Waiting Ends. Careers Begin.
Build job-ready skills. Start applying with confidence.

Turns Gaps into Comebacks
Close skill gaps. Rebuild your career

Break Free. Move Forward
Learn in-demand skills. Take your next career step.

Doubt Out. Confidence In.
Practice real skills. Walk into interviews prepared.

Turn Rejections into Chances
Turn every setback into skills employers value.

Be Smart Learn AI
Learn AI tools. Work smarter. Stay updated

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ABOUT INVENTATEQ

Inventateq is a leading IT training and placement company committed to transforming learners into Industry ready professionals

Our Mission
To deliver high-quality education, practical slots and career opportunities that empower individuals to achieve their dreams

Our Vision
To be a globally recognised training company known for innovation, quality and impactful learner outcomes.

Why Thousands Choose Inventateq?

15+	500+	25,000+	15,000+
Years of Excellence	Hiring Partners	Students Trained	Students Placed

We Collaborate With

Deloitte. · Capgemini · amazon · HCL · Tech Mahindra

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WHY LEARN SYSTEM VERILOG ?

Enterprises worldwide are actively hiring certified System Verilog professionals to drive critical business operations, digital transformation, and modernization.

CAREER SCOPE OF SYSTEM VERILOG

Exponential Industry Demand
Rapid enterprise adoption across global IT firms, MNCs, and technology centers

Premium Salary Compensation
Command competitive compensation packages with rapid growth milestones

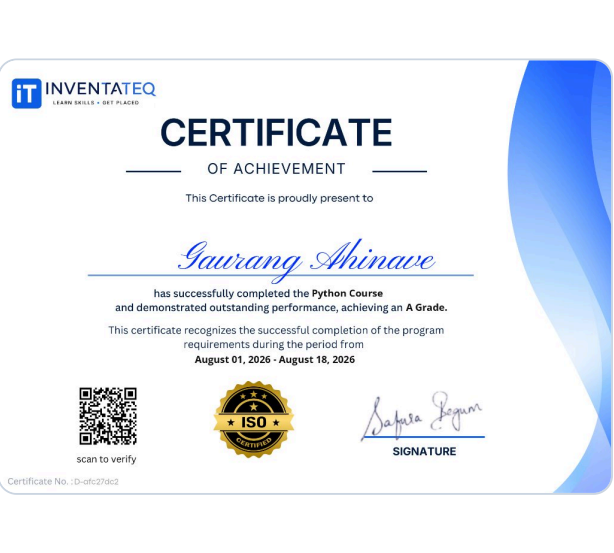
Cross-Industry Opportunities
Versatile skill set applicable across technology, consulting, finance, and core sectors

Future-Proof Career Growth
Long-term job security supported by ongoing digital modernization and tooling investment

Global Certification Pathways
Direct alignment with recognized industry certifications to validate your competence

Worldwide Job Prospects
Open doors to roles in major Indian tech hubs as well as international remote positions

INDUSTRY-RECOGNIZED CERTIFICATION



INVENTATEQ

CERTIFICATE
OF ACHIEVEMENT

This Certificate is proudly present to

Gaurang Ahinave

has successfully completed the Python Course and demonstrated outstanding performance, achieving an A Grade.

This certificate recognizes the successful completion of the program requirements during the period from August 01, 2026 - August 18, 2026

scan to verify

ISO

SIGNATURE

QR Verified · Globally Valid · ISO 9001:2015

Direct Business Impact. Fast-Growing Industry Demand. High Career Mobility.

Average System Verilog Professional Salary in India

₹5.5 LPA – ₹18 LPA

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WHY INVENTATEQ ?

Because we have placed over 15,000+ students and we can place you as well

STUDENT PLACEMENTS

- ✓ 100% Placement Assurance Support
- ✓ 500+ Top Tech Hiring Partners
- ✓ Resume & LinkedIn Optimization
- ✓ Industry Mock Technical Interviews
- ✓ Unlimited Interview Calls Until Placed

COURSE & PLACEMENT VIDEOS

Student Genuine Feedback
Inventateq Reviews & Student Genuine Feed...
Inventateq Bangalore Reviews
Watch Video

Practical Training Success
Autocad Classes in Bangalore, Best Catia Cour...
Industry Tech Career
Watch Video

Placement Story
Ananya's Placement Success Story | AI Course ...
Campus to MNC Offer
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Interview Skills & Growth
Free Interview Skills Development Classes for...
Free Student Masterclass
Watch Video

> **At Inventateq, Your Success is Our Mission !**

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GUARANTEED PLACEMENT SUPPORT

We don't just teach, we prepare you for the real world!

- ✓ Aptitude Training
- ✓ Technical Training
- ✓ Mock Interviews
- ✓ HR Interview Preparation
- ✓ Resume Preparation
- ✓ Cover Letter Preparation
- ✓ LinkedIn Profile Optimisation
- ✓ Job Portal Access
- ✓ Placement Drives & Hiring Events

OUR RECRUITMENT PARTNERS

TATA · Infosys · wipro · Capgemini · Tech Mahindra · LARSEN & TOUBRO · HCL TECH · accenture

OUR PLACEMENT STATS

Our placement record reflects consistent growth, with students securing opportunities across leading companies in diverse industries.

15,000+	500+	95%	6 LPA
Students Placed	Companies Hired	Placement Ratio	Average Package

Check Most Recent Placements

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CAREER PROGRESSION

Job responsibilities, technical competency and portfolio evidence for each role.

ROLE PATHWAY	TYPICAL RESPONSIBILITIES	PORTFOLIO PROOF
System Verilog Associate	Manage core Digital Design tasks, configure tooling, and support delivery.	Practical Digital Design setup files, exercise scripts, and documentation.
System Verilog Specialist	Build practical RTL Modeling workflows, implement features, and resolve issues.	Functional RTL Modeling modules, workflow configs, and practical deliverables.
Senior System Verilog Lead	Lead System Verilog technical delivery, design solutions, and set standards.	Complete System Verilog capstone artifacts, technical blueprints, and reports.

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SKILLS ROADMAP

Progress from core foundations to production-ready enterprise workflows.

MILESTONE	PRACTICAL OUTPUT	REVIEW EVIDENCE
Milestone 1 (Foundations)	Master fundamental Digital Design concepts, environment setup, and tools.	Configured Digital Design workspace and verified practice exercises.
Milestone 2 (Implementation)	Develop practical RTL Modeling workflows and functional domain modules.	Working RTL Modeling project modules and validated practice outputs.
Milestone 3 (Advanced Workflows)	Implement advanced Object-Oriented Verification features, integrations, and optimizations.	Validated Object-Oriented Verification configurations and technical review outputs.
Milestone 4 (Production Capstone)	Deliver an end-to-end System Verilog capstone project and technical review.	Complete System Verilog project portfolio artifact and defense.

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DETAILED MODULE PLAN

10 in-depth modules • 3 Months Duration • Hands-on practical training

1 Module 1: Digital Design and HDL Foundations

- Role of hardware description languages in modern chip design and verification
- Difference between Verilog and
- SystemVerilog in practical project environments
- How digital design, simulation, and verification connect in semiconductor workflows
- Building conceptual clarity before
- syntax-heavy implementation work

GUIDED LAB
Write a basic program to store user information, do simple math, and print the output.

INTERVIEW & ASSESSMENT
Explain the difference between text, numbers, and lists with simple everyday examples.

2 Module 2: SystemVerilog Syntax and Core Data Types

- Variables, nets, logic types, arrays, structures, and enumerations in SystemVerilog
- Using procedural and continuous constructs correctly for hardware modeling
- Understanding strong typing and design clarity in practical coding
- Building readable HDL code for design and verification tasks

GUIDED LAB
Write a basic program to store user information, do simple math, and print the output.

INTERVIEW & ASSESSMENT
Explain the difference between text, numbers, and lists with simple everyday examples.

3 Module 3: RTL Modeling and Design Constructs

- Modeling combinational and sequential logic using always_comb and always_ff
- Using modules, parameters, packages, and generate constructs in scalable RTL
- Building synthesizable code for registers, FSMs, and datapath logic
- Writing design code that supports later verification and debug

GUIDED LAB
Build a simple decision script that checks user input and repeats actions automatically.

INTERVIEW & ASSESSMENT
Explain when to use loops versus if-else conditions in simple words.

4 Module 4: Interfaces, Modports, and Reusability

- Using interfaces to organize connectivity in larger designs
- Understanding modports and signal-direction clarity in modular environments
- Reducing wiring complexity through better code structure
- Improving reuse and readability in block-level design workflows

GUIDED LAB
Complete a guided practical exercise on Using interfaces to organize connectivity and verify your results.

INTERVIEW & ASSESSMENT
Explain the core purpose of Using interfaces to organize connectivity and how you use it in real job roles.

5 Module 5: Simulation and Testbench Foundations

- Difference between synthesizable design code and simulation-only verification code
- Building simple testbenches, clocks, resets, stimulus, and checks
- Using tasks, functions, and procedural control inside verification flow
- Creating disciplined testbench structures for better simulation efficiency

GUIDED LAB
Build a simple decision script that checks user input and repeats actions automatically.

INTERVIEW & ASSESSMENT
Explain when to use loops versus if-else conditions in simple words.

6 Module 6: Object-Oriented Verification Basics

- Classes, objects, inheritance, and
- randomization awareness in verification
- environments
- Applying OOP where it improves reusable verification logic
- Understanding transactions, mailboxes, and verification-side abstraction concepts
- Building the foundation for more advanced methodology-based verification

GUIDED LAB
Build a simple decision script that checks user input and repeats actions automatically.

INTERVIEW & ASSESSMENT
Explain when to use loops versus if-else conditions in simple words.

7 Module 7: Assertions and Functional Checking

- Role of SystemVerilog assertions in design checking and bug detection
- Writing basic properties and checks for protocol or signal behavior
- How assertions improve verification quality and debugging speed
- Connecting assertions to practical functional verification workflows

GUIDED LAB
Build a simple decision script that checks user input and repeats actions automatically.

INTERVIEW & ASSESSMENT
Explain when to use loops versus if-else conditions in simple words.

8 Module 8: Coverage and Verification Metrics Awareness

- Code coverage, functional coverage, and verification-completeness thinking
- Understanding how teams measure
- verification progress and confidence
- Avoiding random testing without measurable verification goals
- Relating coverage thinking to real project closure criteria

GUIDED LAB
Complete a guided practical exercise on Code coverage and verify your results.

INTERVIEW & ASSESSMENT
Explain the core purpose of Code coverage and how you use it in real job roles.

9 Module 9: Design and Verification Workflow Awareness

- How design, simulation, debugging, and verification iterations happen in VLSI projects
- Interview-oriented understanding of RTL, testbench, and assertion usage
- Using SystemVerilog knowledge in design, verification, and support roles
- Positioning SystemVerilog within broader chip-development workflows
- Career Opportunities

GUIDED LAB
Complete a guided practical exercise on How design and verify your results.

INTERVIEW & ASSESSMENT
Explain the core purpose of How design and how you use it in real job roles.

10 Module 10: Real Project Workflow

- Building a small RTL block with corresponding verification logic and checks
- Applying modeling, simulation, assertions, and debugging together
- Preparing project explanation suitable for interviews or academic showcase
- Project output aligned with RTL and
- verification-entry roles
- RTL Design Engineer Trainee
- Verification Engineer Trainee
- VLSI Engineer

GUIDED LAB
Complete an end-to-end practical project bringing together everything you built in this course.

INTERVIEW & ASSESSMENT
Present your completed project and explain your key design decisions with confidence.

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REAL-WORLD PORTFOLIO PROJECTS

Practical industry scenarios, tools applied, and demonstrable project outcomes.

Project 1: verification-entry roles

What it is: Set up the core Digital Design HDL environment and configure essential business settings.

What you do: Initialize base configurations, create clean templates, and verify workflow controls.

Tools used: System Verilog, Digital Design HDL, Role hardware description

Project outcome: Working project foundation configured and tested according to best practices.

Project 2: RTL Design Engineer Trainee

What it is: Build practical RTL Modeling Design modules to handle everyday business operations.

What you do: Create core functional components, validate input data, and prevent common errors.

Tools used: System Verilog, RTL Modeling Design, Modeling combinational sequential

Project outcome: Functional business module ready to run and demo with zero manual errors.

Project 3: Verification Engineer Trainee

What it is: Connect Simulation Testbench with Difference between synthesizable to automate data and team workflows.

What you do: Set up automated pipelines, link required services, and run end-to-end tests.

Tools used: System Verilog, Simulation Testbench, Difference between synthesizable

Project outcome: Live automated workflow pipeline documented with clear usage guides.

Project 4: VLSI Engineer

What it is: Optimize Assertions Functional workflows for security, speed, and reliability.

What you do: Audit performance bottlenecks, apply security rules, and optimize execution speed.

Tools used: System Verilog, Assertions Functional, Role SystemVerilog assertions

Project outcome: Production-grade technical deliverable ready to add to your personal portfolio.

Project 5: System Verilog End-to-End Capstone

What it is: Build a complete, production-ready System Verilog project bringing all skills together.

What you do: Design, code, test, and document a full project workflow from scratch to launch.

Tools used: System Verilog, Design Verification Workflow, design simulation debugging

Project outcome: Verified capstone project ready to showcase on your resume and interview calls.

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ASSESSMENT FRAMEWORK

Module tests, practical evaluations, capstone and completion criteria.

COMPONENT	ASSESSMENT FOCUS	PASS EVIDENCE
Module Knowledge Quizzes	Core Digital Design principles, industry terminology, and workflow concepts	Consistent passing score across syllabus unit evaluation tests
Lab Submissions & Practice Reviews	Hands-on RTL Modeling implementation, configuration, and practical exercises	Working lab deliverables satisfying practical evaluation rubrics
Hands-On Mini Projects	Independent problem-solving using intermediate Object-Oriented Verification techniques	Functional project artifacts addressing realistic domain scenarios
Final Production Capstone	End-to-end System Verilog implementation, quality review, and delivery	Complete capstone submission with technical walkthrough review
Technical Mock Viva	Technical reasoning, troubleshooting approaches, and communication	Successfully defending project decisions in structured mock panels

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RESUME, GITHUB & LINKEDIN

Evidence-based resume writing and professional project presentation.

- Modular GitHub repository per project with setup steps, dependencies, and clean commits.
- Detailed Digital Design diagrams, component specifications, and end-to-end workflows.
- Visual project sheets, live demonstration walkthroughs, and verified functional outputs.
- Project documentation covering RTL Modeling setup, configuration steps, and test notes.
- Direct resume bullet points highlighting hands-on System Verilog tools and technical outcomes.
- Structured practice for technical interview pitches, walkthroughs, and viva defense.

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OUR STUDENT

Meet the learners who turned their goals into successful careers through dedication, skill, and continuous growth.

READ REVIEWS

MS. SNEHA
Placed at Wipro (9.5 LPA)

"The hands-on practical training at Inventateq gave me the exact skills needed to advance my career. The mentors were always available to guide me through complex topics!"
Course Completed : **System Verilog Specialist** ★★★★★

MR. HARSHIT
Placed at Accenture (11.2 LPA)

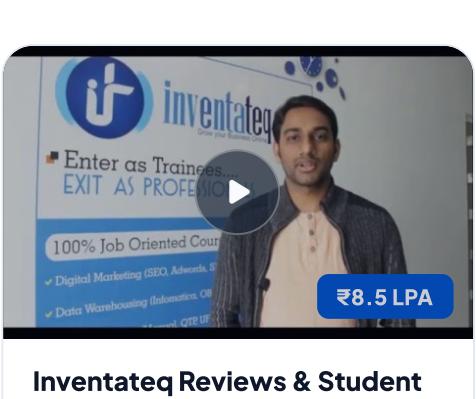
"Inventateq's industry-aligned curriculum and capstone projects set them apart. The mock interviews and placement assistance helped me land my dream offer."
Course Completed : **System Verilog Specialist** ★★★★★

MR. KARTHIK
Placed at Capgemini (10.5 LPA)

"Learning practical enterprise tools with 1-on-1 guidance made all the difference. Having a polished portfolio gave me immense confidence in interviews!"
Course Completed : **System Verilog Specialist** ★★★★★

WATCH VIDEOS

Watch real stories from our students as they talk about their journey, growth, and placement success.



Inventateq Reviews & Student Genuine Feedback Bangalore
Course Video 1 • Student Feedback
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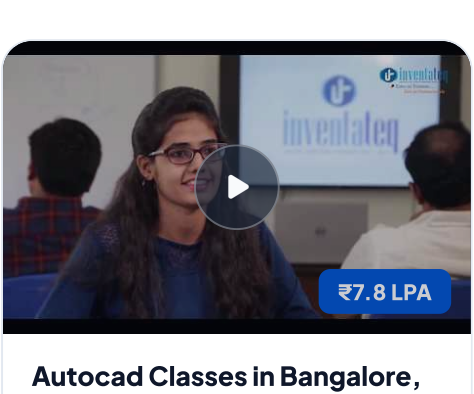

Autocad Classes in Bangalore, Best Catia Course Near Me with Job Support
Course Video 2 • Student Feedback
Watch Story

Ananya's Placement Success Story | AI Course | 6.5 LPA at Accenture| Inventateq
Course Video 3 • Student Feedback
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Classes @ INVENTATEQ.COM
₹6.8 LPA

Free Interview Skills Development Classes for Freshers & College Students
Course Video 4 • Student Feedback
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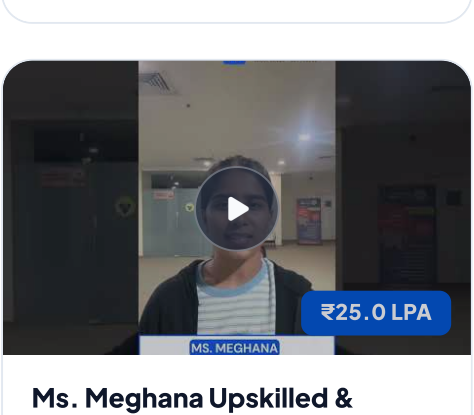
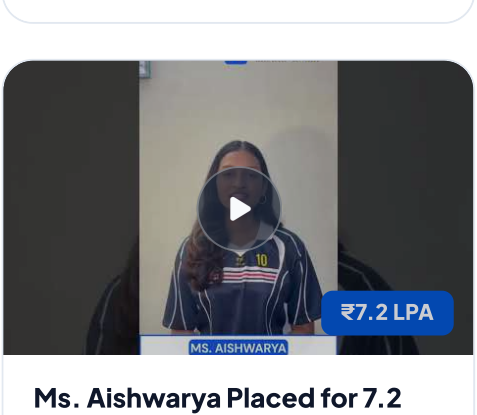


Ms. Meghana Upskilled & Placed at 25 LPA
Top Offer • Enterprise Consultant
Watch Story



Ms. Aishwarya Placed for 7.2 LPA Package
Verified Offer • Software Dev
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